**Board Assembly and Testing**

**Engineering 155 Lab I Report**

**September 7th, 2021**

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**Introduction:**

The goal of this lab was to assemble and test the µMudd Mark IV boards and test them with the Nucleo F401RE MCU and MAX1000 FPGA boards. We were to solder the boards with the appropriate components (header pins, resistor networks, dip switches, etc.) before programming the FPGA with Verilog code and interfacing a seven-segment display to the board which showed a single hexadecimal digit corresponding to the input on the switches.

**Design Methodology:**

In designing the hardware for the system, the main point of concern was the maximum current that the 7-segment display could handle. Consultation of the UA5651-11EWRS datasheet made it known that the acceptable range for current through the component is between 5 and 20mA. For simplicity of calculation, 10mA was chosen. The 3.3V power source on the µMudd Mark IV was used to power the component, and so it was found that a 330-ohm resistor was necessary to limit the current to 10mA as shown in Figure 1 below.

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Fig. 1: Calculation for strength of resistor

In designing the software for the system, two SystemVerilog modules were created using Quartus. One main module for calculating outputs of LEDs and segments of the 7-segment display and one counter module aiding in blinking an LED at 2.4Hz. The given parameters for the software portion are outlined in Figure 3 below.

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Fig. 3: Given parameters for the main module

The input clk was driven by the FPGA’s built-in 12MHz clock, and the input was taken in by assigning the correct pin on the board to drive the bit. We used the clk input to blink LED 7 at 2.4Hz using a divide-by-2N counter whose implementation will be discussed later. However, using the equation fout = fclk \* (p / 2N), it was found that the combination of p = 214, N = 30 gives an accurate approximation of 2.4Hz.

Each bit of the output seg[6:0] corresponded to one of the segments in the display, which was to display a single hexadecimal digit specified by the input s[3:0]. The logic for led[7:0] is shown in Figure 4 below.

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Fig. 4: Logic for the output of each LED

Testing of the software component was conducted by simulating the logic in ModelSim. By using the force command in the simulation terminal, every case for was tested and was found to yield the correct result for both the seg[6:0] and led[7:0] outputs.

**Technical Documentation:**

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Fig. 5: SystemVerilog code

On the previous page is the SystemVerilog code used to operate the system, and below is the logical circuit diagram associated with it.

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Fig. 6: RTL schematic showing logic elements

**Table

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Fig. 7: Pin placements

Diagram, schematic

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Fig. 8: Circuit schematic

**Results and Discussion:**

I was successful in accomplishing all the prescribed tasks. The board’s LEDs lit up properly and every possible digit was tested and successful.

If I were to redo this lab, I would solder my board correctly the first time. I had a nightmare resoldering my board for hours on end.

**Conclusion:**

I was successful in assembling and testing my board. I successfully interfaced a 7-segment display to the board controlled by the DIP switches I soldered onto the board. The system performed as I had hoped, and I was able to get it to work perfectly by the end of the lab.

**This lab took 16 hours to complete, and the report alone took 4 hours. I fear I have no choice but to become a basement-dwelling troll this semester…**

**As for the future, I think the lab could be a little more thoroughly explained. I spent a lot of confused over instructions I felt were unclear and found myself frequently needing the help of proctors.**